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EXAMINER	
TORRES, JUAN A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.**	**Applicant(s)**	
	09/729,443	JAFFE ET AL.	
	Examiner	**Art Unit**	
	JUAN A. TORRES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *62-115* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *62-115* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/26/2007 has been entered.

Drawings

The modifications to the drawings were received on 11/26/2007. These modifications are accepted by the Examiner.

In view of the amendment filed on 11/26/2007, the Examiner withdraws Drawing objections of the previous Office action.

Claim Rejections - 35 USC § 112

In view of the amendment filed on 11/26/2007, the Examiner withdraws claim rejections under 35 USC § 112 first paragraph to claims 62-115 of the previous Office action.

Claims 62-115 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In the present Application, the decoder, is comprised by a Viterbi decoder (that will decode the signal from the first trellis encoder (203) to produce carrier synchronization) in series with a turbo decoder.

The Viterbi decoder produces a decoded signal that will be "the quantized symbol", that is the ideally symbol that was sent in the mapped constellation point in the transmitter. The Viterbi decoder will make a hard decision to see the error in the received signal; with the received signal and the decoded signal from the Viterbi decoder we can see the difference that will be representative of the error in the received signal, and with this error we control the carrier in the receiver so that the error is minimized.

The Viterbi decoder produce a decoded signal that is a quantized signal located in the ideal transmitted point.

The Viterbi decoder also has a switch to avoid that signals coming from the second trellis encoder (207) reach the Viterbi decoder, for this reason the signals from the second Viterbi decoder do not enter the Viterbi decoder, <u>and consequently they will not enter the turbo decoder</u>.

The disclosure and/or claims don't enable to one skill in the art how the turbo decoder will decode a signal that has already been decoded by the Viterbi decoder.

The disclosure and/or claims don't enable to one skill in the art how the turbo decoder will decode a signal that has already been decoded by the Viterbi decoder and that doesn't provide information about the second encoder, because the switch will be

open when the signal from the second encoder is received, therefor the signal from the second encoder doesn’t enter the receiver.

Response to Arguments

Regarding claims 62, 72, 82, 91, 99, 106 and 113:

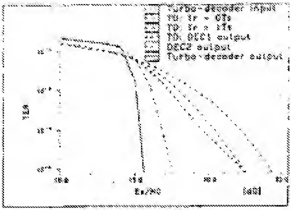
Applicant's arguments filed 11/26/2007 have been fully considered but they are not persuasive.

The Applicant contends:

> “The Applicant respectfully believes that Mottier fails to teach and disclose any such limitation of a "Viterbi decoder operating with a zero traceback depth", "Viterbi decoding operating with a zero traceback depth", a "Viterbi decoder operating with less than a full traceback depth" and/or "Viterbi decoding operating with less than a full traceback depth". In other words, the Applicant respectfully believes that Mottier fails to teach and disclose any such limitation of any limited (e.g., less than full) and/or zero "traceback depth" employed within a Viterbi decoder or Viterbi decoding. As such, the Applicant respectfully asserts that Mottier fails to teach and disclose each and every element of the subject matter as claimed by the Applicant in these rejected claims”

The Examiner disagrees, and asserts that, Mottier discloses in section 3.1 specifically that “Therefore, the mean BER of the bit sequence used to build a symbol tentative decision d(k) depends on the BER of the bit tentative decisions extracted from DEC1 and on the BER before decoding, each weighted by a coefficient depending on the puncturing matrix. <u>The BER. of the bit tentative decisions issued from DEC1 is presented FIC.4 for a 64-QAM with Re = 1/2 and 2/3 coding rate. Tile curves are plotted for different values of symbol delay</u>. Regardingformance reference, the BER curve after 1 iteration of Turbo-decoding is presented”

Figure 4 shows:



(b) $R_c = 2/3$

Fig. 4. Delay influence on tentative decisions (TD) reliability.

Figure 4b shows performance for a delay of zero Tr=0 Ts, so in fact Mottier is disclosing a Viterbi decoder with delay zero, so it is a Viterbi decoder that doesn't depend of future values of the signal. In section 3.2 "Delay insertion" Mottier also discloses that the values for Tr=0 are possible (see equation 5)

So it is clear from this presentation that the reference of Mottier clearly anticipated the idea of the present invention.

So after a very carefully review and consideration of the specification and drawings of the present application and the reference used for the rejection it is clear the rejection is proper and should be maintained.

It is also important to considerate the reference of Mottier also provide detail simulations of the performance of the system in comparison with slicer, Viterbi decoder with a delay of zero and also using the output of the turbo coder.

For these reasons and the reason stated in the previous Office Action, the rejection of claims 62, 72, 82, 91, 99, 106 and 113 are maintained.

<u>Regarding claims 63-71, 73-81, 83-90, 92-98, 100-105, 107-112 and 114-115:</u>

Applicant's arguments filed 11/26/2007 have been fully considered but they are not persuasive.

The Applicant contends:

> “The Applicant respectfully believes that these dependent claims rejected above, being further limitations of the subject matter as claimed in allowable independent claims, respectively, are also allowable. As such, the Applicant respectfully requests that the Examiner withdraw the rejections of these claims under 35 U.S.C. § 102(b) as being anticipated by Mottier. Claim Rejections - 35 U.S.C. § 103 In the final office action, the Examiner states: "Claims 68, 70, 71, 78, 80, 81, 87, 89, 90, 95, 97, 98, 102, 104, 105, 109, 111, 112, 114 and 115 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mottier as applied to claims 62, 72 and 82 above, and further in view of Applicant Admitted Prior Art (AAPA)." (final office action, Part of Part of Paper No./Mail Date 20070831, p. 25). The Applicant respectfully traverses. The Applicant has amended certain of the claims. The Applicant's comments made above are also applicable here. The Applicant respectfully asserts that Mottier and the Examiner's characterized "AAPA", when considered individually or together, fails to teach and disclose the subject matter as claimed by the Applicant in these claims. As such, the Applicant respectfully requests that the Examiner withdraw the rejection of these claims under 35 U.S.C. § 103(a) as being unpatentable over Mottier as applied to claims 62, 72 and 82 above, and further in view of Applicant Admitted Prior Art (AAPA) ”

The Examiner disagrees, and asserts that, because the rejection of claims 62, 72, 82, 91, 99, 106 and 113 are maintained, the rejection of claims 63-71, 73-81, 83-90, 92-98, 100-105, 107-112 and 114-115 are also maintained.

For these reasons and the reason stated in the previous Office Action, the rejection of claims 63-71, 73-81, 83-90, 92-98, 100-105, 107-112 and 114-115 are maintained.

Claim Rejections - 35 USC § 101

Claims 62-115 are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility.

In the present Application, the decoder, is comprised by a Viterbi decoder (that will decode the signal from the first trellis encoder (203) to produce carrier synchronization) in series with a turbo decoder.

The Viterbi decoder produces a decoded signal that will be "the quantized symbol", that is the ideally symbol that was sent in the mapped constellation point in the transmitter. The Viterbi decoder will make a hard decision to see the error in the received signal; with the received signal and the decoded signal from the Viterbi decoder we can see the difference that will be representative of the error in the received signal, and with this error we control the carrier in the receiver so that the error is minimized.

The Viterbi decoder produce a decoded signal that is a quantized signal located in the ideal transmitted point.

The Viterbi decoder also has a switch to avoid that signals coming from the second trellis encoder (207) reach the Viterbi decoder, for this reason the signals from the second Viterbi decoder do not enter the Viterbi decoder, and consequently they will not enter the turbo decoder.

The present 35 USC 101 rejection is based in that the device will not be operative, because the input of the turbo decoder (output of the Viterbi decoder) is already a decoded signal from the Viterbi decoder, centered in the ideal transmitted constellation point, for this reason the turbo decoder will not work, because the input is the ideal transmitted signal; and also, because the turbo decoder doesn't have information about the second trellis encoder, due to the open switch.

Regarding claim 62, the recitation in line 10-12 of claim 62 “a turbo decoder that is operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein” is inoperative, because the synchronization module, that includes the Viterbi decoder will provide the already decoded signal (first, second, third and fourth signals), centered in the ideal transmitted point, and the turbo decoder will not work (see discussion immediately above).

Regarding claims 63-71, they are rejected because they depend directly from claim 62, and claim 62 is rejected.

Regarding claim 72, the recitation in lines 10-11 of claim 72 “turbo decoding the first symbol, the second symbol, and the third symbol that are recovered from the signal to make best estimates of information bits encoded therein” is inoperative, because the Viterbi decoder will provide the already decoded first signal centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

Regarding claims 73-81, they are rejected because they depend directly from claim 72, and claim 72 is rejected.

Regarding claim 82, the recitation in lines 17-19 of claim 82 “a turbo decoder that is operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein” is inoperative, because the Viterbi decoder will provide the already decoded first signal centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

Regarding claims 83-90, they are rejected because they depend directly from claim 82, and claim 82 is rejected.

Regarding claim 91, the recitation in lines 17-18 of claim 91 “turbo decoding the first symbol, the second symbol, and the third symbol that are recovered from the signal to make best estimates of information bits encoded therein” is inoperative, because the Viterbi decoder will provide the already decoded first signal centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

Regarding claims 92-98, they are rejected because they depend directly from claim 91, and claim 91 is rejected.

Regarding claim 99, the recitation in lines 26-28 of claim 99 “a turbo decoder that 1s operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein” is inoperative, because the Viterbi decoder will provide the already decoded first signal centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

Regarding claims 100-105, they are rejected because they depend directly from claim 99, and claim 99 is rejected.

Regarding claim 106, the recitation in lines 21-22 of claim 106 “turbo decoding the first symbol, the second symbol, and the third symbol that are recovered from the signal.” is inoperative, because the Viterbi decoder will provide the already decoded first signal centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

Regarding claims 107-112, they are rejected because they depend directly from claim 106, and claim 106 is rejected.

Regarding claim 113, the recitation in lines 27-29 of claim 113 “a turbo decoder that is operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein” is inoperative, because the Viterbi decoder will provide the already decoded first signal centered in the ideal transmitted point, and the turbo decoder will not work (see discussion above).

Regarding claims 114-115, they are rejected because they depend directly from claim 113, and claim 113 is rejected.

Claim Objections

Claims 62-71 are objected to because of the following informalities:

Regarding claim 62, the recitation in line 7 of claim 62 “second symbol; and” is improper, because it is not properly constructed (see line 7 of claim 72); it is suggested to be changed to “second symbol;”

Regarding claims 63-71, they are objected because they depend directly from claim 62, and claim 62 is objected.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 62-67, 72-77, 82-86, 91-94, 99-101 106-108 and 113 are rejected under 35 U.S.C. 102(b) as being anticipated by Mottier ("Influence of tentative decisions provided by a Turbo-decoder on the carrier synchronization: Application to 64-QAM signals", COST 254 Workshop on Emerging Techniques for Communication Terminals, Toulouse France July 7-9, 1997, pages 326-330).

Regarding claims 62 and 72, Mottier discloses an input, coupled to a communication channel, that is operable to receive a signal (figure 3 y(k) sections 2 and 3, pages 327-328); a synchronization module that includes a Viterbi decoder, a phase detector, and a voltage controlled oscillator, wherein the synchronization module is operable to recover a first symbol, a second symbol, and a third symbol from the signal (figure 3 sections 2 and 3, pages 327-328); the first symbol is followed by the second symbol (figure 3 sections 2 and 3, pages 327-328); and the second symbol is followed by the third symbol (figure 3 sections 2 and 3, pages 327-328); the Viterbi decoder operating with a zero traceback depth (section 3.1 and 3.2 Tr=0 see response to arguments above); and a turbo decoder that is operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein (figure 3 "turbo decoder" sections 2 and 3, pages 327-328).

Regarding claims 63 and 73, Mottier discloses claims 62 and 72, Mottier also discloses a multiplier, whose mixing frequency is governed by the voltage controlled oscillator, that is operable to multiply the signal by the mixing frequency to match a

carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal frequency (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k)).

Regarding claims 64 and 74, Mottier discloses claims 62 and 72, Mottier also discloses that the Viterbi decoder is operable to consider the first symbol when estimating the second symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 “A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)”); and the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 “A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)”).

Regarding claims 65 and 75, Mottier discloses claims 62 and 72, Mottier also discloses a multiplier, whose mixing frequency is governed by the voltage controlled oscillator, that is operable to multiply the signal by the mixing frequency to match a

carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k)); and wherein: the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); and the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, Regardingformed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 "phase detector").

Regarding claims 66 and 76, Mottier discloses claims 62 and 72, Mottier also discloses a multiplier, whose mixing frequency is governed by the voltage controlled oscillator, that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k)); and wherein: the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2

and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 "phase detector"); and the adjustment of the voltage controlled oscillator is operable to make the mixing frequency to be substantially equal to the carrier frequency of the signal (figure 3 sections 2 and 3, pages 327-328 output of the phase detector).

Regarding claims 67 and 77, Mottier discloses claims 62 and 72, Mottier also discloses a multiplier, whose mixing frequency is governed by the voltage controlled oscillator, that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k)); and wherein the third symbol output from the multiplier is provided simultaneously to both the Viterbi decoder and the phase detector (figure 3 sections 2 and 3, pages 327-328 after multiplier after y(k) the symbols are provided to the phase detector and to the Viterbi decoder); the Viterbi decoder is operable to consider the first

symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder); and the phase detector is operable to compare the third symbol output from the multiplier and the estimate of the third symbol as made by the Viterbi decoder to determine whether recovery of symbols from the signal, performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 phase detector).

Regarding claim 82, Mottier discloses an input, coupled to a communication channel, that is operable to receive a signal (figure 3 y(k) sections 2 and 3, pages 327-328); a multiplier that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k)); a synchronization module that includes a Viterbi decoder, a phase detector, and a voltage controlled oscillator (figure 3 sections 2 and 3, pages 327-328), wherein: the Viterbi decoder and the phase detector each receive the mixed signal output from the multiplier (figure 3 sections 2 and 3, pages 327-328 output of the multiplier); the synchronization module is operable to recover a first symbol, a second symbol, and a third symbol from the signal (figure 3 sections 2 and 3, pages 327-328); the first symbol is followed by the second symbol, the second symbol is followed by the third symbol (figure 3 sections 2 and 3, pages 327-328); and the mixing frequency of the multiplier is governed by the voltage controlled oscillator (figure 3 sections 2 and 3, pages 327-328); the Viterbi decoder operating with a zero traceback depth (section 3.1

and 3.2 Tr=0 see response to arguments above); and a turbo decoder that is operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein (figure 3 sections 2 and 3, pages 327-328 turbo decoder).

Regarding claim 83, Mottier discloses claim 82, Mottier also discloses that the Viterbi decoder is operable to consider the first symbol when estimating the second symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 “A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)”); and the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 “A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)”).

Regarding claim 84, Mottier discloses claim 82, Mottier also discloses that the Viterbi decoder is operable to consider the first symbol and the second symbol when

estimating the third symbol (figure 3 sections 2 and 3, pages 327-328); and the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 “phase detector”).

Regarding claim 85, Mottier discloses claim 82, Mottier also discloses that the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 “A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)”); the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 “phase detector”); and the adjustment of the voltage controlled oscillator is operable to make the mixing frequency to be substantially equal to the carrier frequency of the signal (figure 3 sections 2 and 3, pages 327-328 output of the phase detector).

Regarding claim 86, Mottier discloses claim 82, Mottier also discloses that the third symbol output from the multiplier is provided simultaneously to both the Viterbi decoder and the phase detector (figure 3 sections 2 and 3, pages 327-328 after multiplier after y(k) the symbols are provided to the phase detector and to the Viterbi decoder); the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder); and the phase detector is operable to compare the third symbol output from the multiplier and the estimate of the third symbol as made by the Viterbi decoder to determine whether recovery of symbols from the signal, performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 phase detector).

Regarding claim 91, Mottier discloses receiving a signal from a communication channel (figure 3 y(k) sections 2 and 3, pages 327-328); recovering a first symbol, a second symbol, and a third symbol from the signal from the signal by multiplying the signal by a mixing frequency to match a carrier frequency of the signal and subsequent Viterbi decoding and phase detection of symbols generated by the frequency mixing (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k), Viterbi decoder and phase detector), wherein: the multiplied signal is simultaneously provided for Viterbi decoding and phase detection (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k), Viterbi decoder and phase detector); the first symbol is followed by the second symbol (figure 3 sections 2 and 3, pages 327-328); and the second symbol is followed

by the third symbol (figure 3 sections 2 and 3, pages 327-328 multiplier after y(k), Viterbi decoder and phase detector); and when performing Viterbi decoding, considering the first symbol when estimating the second symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]); the Viterbi decoder operating with a zero traceback depth (section 3.1 and 3.2 Tr=0 see response to arguments above); when performing Viterbi decoding, considering the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328); and turbo decoding the first symbol, the second symbol, and the third symbol that are recovered from the signal to make best estimates of information bits encoded therein (figure 3 sections 2 and 3, pages 327-328 turbo decoder).

Regarding claim 92, Mottier discloses claim 91, Mottier also discloses employing at least one of the first symbol, the second symbol, and the third symbol when performing phase detection to determine whether recovery of symbols from the signal is lagging or leading actual symbols within the signal (figure 3 sections 2 and 3, pages 327-328 phase detector, multiplier, Viterbi decoder); and adjusting the mixing frequency based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 phase detector).

Regarding claim 93, Mottier discloses claim 91, Mottier also discloses employing at least one of the first symbol, the second symbol, and the third symbol when performing phase detection to determine whether recovery of symbols from the signal is

lagging or leading actual symbols within the signal (figure 3 sections 2 and 3, pages 327-328 phase detector, multiplier, Viterbi decoder); adjusting the mixing frequency based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 phase detector); and wherein: the adjustment of the mixing frequency is operable to make the mixing frequency to be substantially equal to the carrier frequency, of the signal (figure 3 sections 2 and 3, pages 327-328 carrier synchronization).

Regarding claim 94, Mottier discloses claim 91, Mottier also discloses when performing phase detection, comparing the third symbol output from the multiplying and the estimate of the third symbol as made in accordance with Viterbi decoding to determine whether recovery of symbols from the signal is lagging or leading actual symbols within the signal (figure 3 sections 2 and 3, pages 327-328 phase detector, multiplier and Viterbi decoder); and adjusting the mixing frequency based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 carrier synchronization).

Regarding claims 99 and 106, Mottier discloses an input, coupled to a communication channel, that is operable to receive a signal (figure 3 y(k) sections 2 and 3, pages 327-328); a multiplier that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 multiplier after y(k) sections 2 and 3, pages 327-328); a synchronization module that includes a Viterbi decoder, a phase detector, and a voltage controlled oscillator (figure 3 multiplier, Viterbi decoder, phase detector, pages 327-328), wherein: the Viterbi decoder and the phase detector each receive the mixed signal output from the multiplier (figure 3 output

multiplier input to Viterbi decoder and phase detector, pages 327-328); the synchronization module is operable to recover a first symbol, a second symbol, and a third symbol from the signal (figure 3 multiplier, Viterbi decoder, phase detector, pages 327-328); the first symbol is followed by the second symbol (figure 3 pages 327-328); the second symbol is followed by the third symbol (figure 3 pages 327-328); the mixing frequency of the multiplier is governed by the voltage controlled oscillator (figure 3 pages 327-328); the Viterbi decoder is operable to consider the first symbol when estimating the second symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 “A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)”); the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328, see above); the Viterbi decoder operating with a zero traceback depth (section 3.1 and 3.2 Tr=0 see response to arguments above); and the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of symbols from the signal, Regardingformed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 sections 2 and 3, pages 327-328 carrier synchronization); and a turbo decoder that is operable to decode the

first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein (figure 3 sections 2 and 3, pages 327-328 turbo decoder).

Regarding claims 100 and 107, Mottier discloses claims 99 and 106, Mottier also discloses that the adjustment of the voltage controlled oscillator is operable to make the mixing frequency to be substantially equal to the carrier frequency of the signal (figure 3 sections 2 and 3, pages 327-328 carrier synchronization).

Regarding claims 101 and 108, Mottier discloses claims 99 and 106, Mottier also discloses that the third symbol output from the multiplier is provided simultaneously to both the Viterbi decoder and the phase detector (figure 3 sections 2 and 3, pages 327-328 output of the multiplier to the phase detector and the Viterbi decoder).

Regarding claim 113, Mottier discloses an input, coupled to a communication channel, that is operable to receive a signal (figure 3 y(k) sections 2 and 3, pages 327-328); a multiplier that is operable to multiply the signal by the mixing frequency to match a carrier frequency of the signal to assist in recovery of the first symbol, the second symbol, and the third symbol from the signal (figure 3 multiplier sections 2 and 3, pages 327-328); a synchronization module that includes a Viterbi decoder, a phase detector, and a voltage controlled oscillator (figure 3 multiplier, Viterbi decoder and phase detector sections 2 and 3, pages 327-328), wherein: the Viterbi decoder and the phase detector each receive the mixed signal output from the multiplier (figure 3 the output of the multiplier is sent to the Viterbi decoder and the phase detector sections 2 and 3, pages 327-328); the output of the Viterbi decoder is provided to the phase detector

(figure 3 output of Viterbi decoder is sent to the other input of the phase detector sections 2 and 3, pages 327-328); the synchronization module is operable to recover a first symbol, a second symbol, and a third symbol from the signal such that the first symbol is followed by the second symbol and the second symbol is followed by the third symbol (figure 3 y(k) sections 2 and 3, pages 327-328); the Viterbi decoder is operable to consider the first symbol when estimating the second symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); and the Viterbi decoder is operable to consider the first symbol and the second symbol when estimating the third symbol (figure 3 sections 2 and 3, pages 327-328 this is inherent to a Viterbi decoder, see in figures 1, 2 and 3 how each state of the Viterbi decoder depends of the previous states [dotted line inside of the Viterbi decoder]. This is also acknowledged by the Applicant in page 4 lines 23-25 "A Viterbi decoder uses the past and future data as well as correlations within the data to produce a current symbol that is more likely to be correct than if only the present data is used (such as with a typical data slicer)"); the Viterbi decoder operating with a zero traceback depth (section 3.1 and 3.2 Tr=0 see response to arguments above); the phase detector is operable to employ at least one of the first symbol, the second symbol, and the third symbol to determine whether recovery of

symbols from the signal, performed by the synchronization module, is lagging or leading actual symbols within the signal and to adjust the voltage controlled oscillator based on any lagging or leading (figure 3 carrier synchronization sections 2 and 3, pages 327-328); and the adjustment of the mixing frequency by the voltage controlled oscillator is operable to make the mixing frequency to be substantially equal to the carrier frequency of the signal (figure 3 carrier synchronization sections 2 and 3, pages 327-328); and a turbo decoder that is operable to decode the first symbol, the second symbol, and the third symbol that are provided from the synchronization module to make best estimates of information bits encoded therein (figure 3 turbo decoder sections 2 and 3, pages 327-328).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 68, 70, 71, 78, 80, 81, 87, 89, 90, 95, 97, 98, 102, 104, 105, 109, 111, 112, 114 and 115 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mottier as applied to claims 62, 72 and 82 above, and further in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 68, 78, 87, 95, 102, 109 and 114, Mottier discloses claims 62, 72, 82, 91, 99, 106 and 113, Mottier doesn't specifically disclose that the communication device is coupled to at least one additional communication device via the

communication channel; the at least one additional communication device includes a turbo encoder that is operable to encode at least one information bit thereby generating at least one of the first symbol, the second symbol, and the third symbol of the signal; and the at least one additional communication device is operable to launch the signal into the communication channel. AAPA discloses that the communication device is coupled to at least one additional communication device via the communication channel (figure 2 page 3 line 34 to page 4 line 6); the at least one additional communication device includes a turbo encoder that is operable to encode at least one information bit thereby generating at least one of the first symbol, the second symbol, and the third symbol of the signal (figure 2 page 3 line 34 to page 4 line 6); and the at least one additional communication device is operable to launch the signal into the communication channel (figure 2 page 3 line 34 to page 4 line 6). Mottier and AAPA teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the carrier synchronization technique disclosed by Mottier with the system discloses by AAPA. The suggestion/motivation for doing so would have been to use and effective synchronization at very low SNR (Mottier abstract).

Regarding claims 70, 80, 89, 97, 104, 111 and 115, Mottier discloses claims 62, 72, 82, 91, 96, 106 and 113, Mottier doesn't specifically disclose that the signal is received by the communication device via a communication channel that couples the communication device to a relay satellite. AAPA discloses that the signal is received by

the communication device via a communication channel that couples the communication device to a relay satellite (figures 1 page 3 lines 15-24). Mottier and AAPA teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the carrier synchronization technique disclosed by Mottier with the system discloses by AAPA. The suggestion/motivation for doing so would have been to use and effective synchronization at very low SNR (Mottier abstract).

Regarding claims 71, 81, 90, 98, 105 and 112, Mottier discloses claims 62, 72, 82, 91, 99 and 106, Mottier doesn't specifically disclose that the communication device is coupled to at least one additional communication device via the communication channel (figures 1 page 3 lines 15-24); the communication channel includes a relay satellite (figures 1 page 3 lines 15-24); the communication device is a satellite communication receiver (figures 1 page 3 lines 15-24); and the at least one additional communication device is a communication transmitter (figures 1 page 3 lines 15-24). Mottier and AAPA teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the carrier synchronization technique disclosed by Mottier with the system discloses by AAPA. The suggestion/motivation for doing so would have been to use and effective synchronization at very low SNR (Mottier abstract).

Claims 69, 79, 88, 96, 103, 110 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mottier as applied to claims 62 and 72 above, in view of AAPA, and further in view of Robertson et al., “Bandwidth-Efficient Turbo Trellis-coded Modulation Using Punctured Component Codes," IEEE Journal on Selected Areas in Communications; 02/1998,.p.p. 206-218,. Vol. 16, No. 2).

Regarding claims 69, 79, 88, 96, 103 and 110, Mottier discloses claims 62, 72, 82, 91, 96 and 106, Mottier doesn’t specifically disclose that the communication device is coupled to at least one additional communication device via the communication channel; the at least one additional communication device includes a turbo encoder that is operable to encode data thereby generating the first symbol, the second symbol, and the third symbol of the signal; the turbo encoder includes: a first trellis encoder that is operable to encode the data thereby generating first encoded data; an interleaver that is operable to interleave the data thereby generating interleaved data; a second trellis encoder that is operable to encode the interleaved data thereby generating interleaved encoded data; an inverse interleaver that is operable to unscramble the interleaved encoded data that has been generated by the second trellis encoder thereby generating second encoded data; a switch that is operable alternatively to select symbols from the first encoded data and the second encoded data; and the at least one additional communication device is operable to launch the signal into the communication channel. AAPA discloses the communication device is coupled to at least one additional communication device via the communication channel (figure 2 page 3 line 34 to page 4 line 6); the at least one additional communication device includes a turbo encoder that

is operable to encode data thereby generating the first symbol, the second symbol, and the third symbol of the signal (figure 2 page 3 line 34 to page 4 line 6); the turbo encoder includes: a first trellis encoder that is operable to encode the data thereby generating first encoded data (figure 2 page 3 line 34 to page 4 line 6); an interleaver that is operable to interleave the data thereby generating interleaved data (figure 2 page 3 line 34 to page 4 line 6); a second trellis encoder that is operable to encode the interleaved data thereby generating interleaved encoded data (figure 2 page 3 line 34 to page 4 line 6); a switch that is operable alternatively to select symbols from the first encoded data and the second encoded data (figure 2 page 3 line 34 to page 4 line 6); and the at least one additional communication device is operable to launch the signal into the communication channel (figure 2 page 3 line 34 to page 4 line 6). Mottier and AAPA teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the carrier synchronization technique disclosed by Mottier with the system discloses by AAPA. The suggestion/motivation for doing so would have been to use and effective synchronization at very low SNR (Mottier abstract). Robertson teaches that the turbo-coded transmitted signals comprise interleaving and de-interleaving of the turbo encoded signals before transmission (figure 2 and 2 page 208 section II the encoder). Mottier, AAPA and Roberson teachings are analogous art because they are from the same field of endeavor of carrier synchronization. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the interleaving and de-interleaving of the turbo

encoded signals before transmission disclosed by Roberson with the carrier recovery scheme disclosed by Mottier and AAPA. The suggestion/motivation for doing so would have been to ensure that the ordering of the two information bits partly defining each symbol corresponds to that of the first encoder (Roberson page 208 section II. A) and to reduce the latency of the turbo decoder.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Huff (US 5974091 A) discloses a composite trellis system and method using a zero traceback Viterbi to reduce complexity and delay

b) Huff (US 6477208 B1) discloses a composite trellis system and method using a zero traceback Viterbi to reduce complexity and delay

c) Eyuboglu (US 4833693 A) discloses a Viterbi decoder 50 with output with different tracebacks.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Juan Alberto Torres
04-14-2008

/Juan A Torres/

Examiner, Art Unit 2611